

PRODUCT SPECIFICATION

Doc. Number:

- Tentative Specification
- Preliminary Specification
- Approval Specification

MODEL NO.: N173HGE
SUFFIX: E11

Customer:**APPROVED BY****SIGNATURE****Name / Title**

Note

Please return 1 copy for your confirmation with your
signature and comments.

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REVISION HISTORY

Version	Date	Page	Description
0.0	Dec.28, 2012	All	Spec Ver.0.0 was first issued.
1.0	Mar.15, 2013	All	Spec Ver.1.0 was first issued.
2.0	Apr.22, 2013	All	Spec Ver.2.0 was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N173HGE-E11 is a 17.3" TFT Liquid Crystal Display module with LED Backlight unit and 30 pins eDP interface. This module supports 1920 x 1080 FHD model and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	17.3" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.1989 (H) x 0.1989 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	300	Cd/m ²	
Power Consumption	Total 8.3W (Max.) @ cell 1.9W (Max.), BL 6.4W (Max.)		

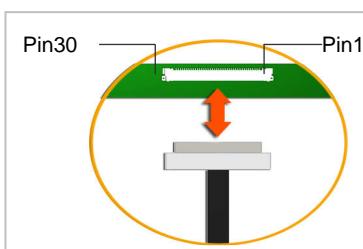
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	397.6	398.1	mm	(1)
	Vertical (V)	232.3	232.8	mm	
	Thickness (T)	-	5.7	6.0	
Bezel Area	Horizontal	385.88	386.18	mm	
	Vertical	218.55	218.85	mm	
Active Area	Horizontal	-	381.888	mm	
	Vertical	-	214.812	mm	
Glass	CF	0.45	0.5	0.55	mm
Thickness	TFT	0.45	0.5	0.55	mm
Weight		-	555	570	g

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12 or equivalent

User's connector Part No: IPEX-20453-030T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

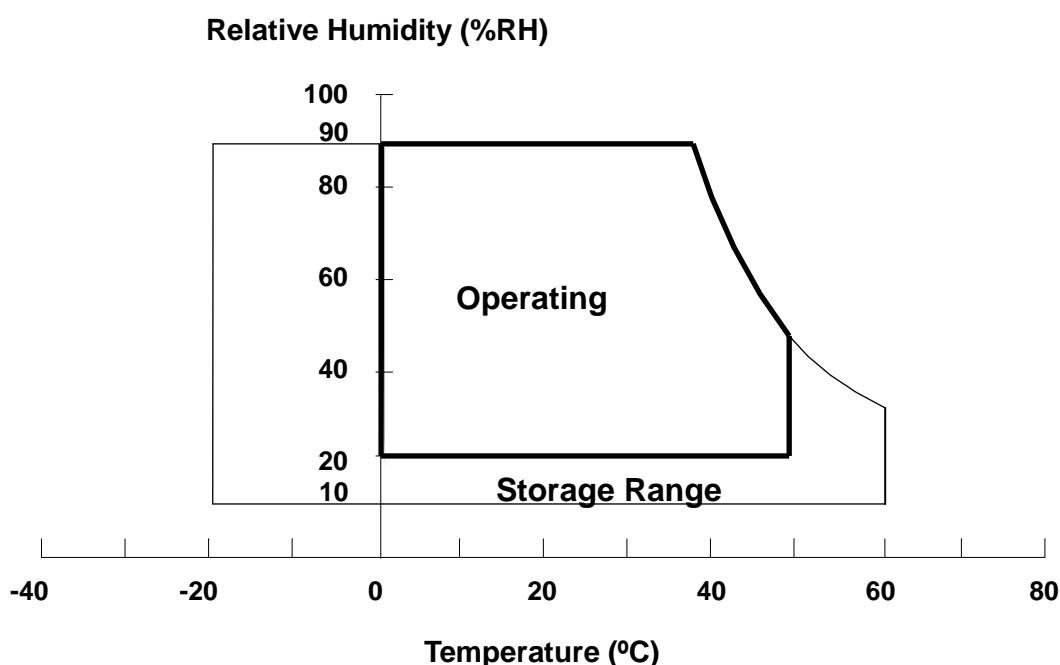
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T_{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. ($T_a \leq 40^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40^{\circ}\text{C}$).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



3.2 ELECTRICAL ABSOLUTE RATINGS

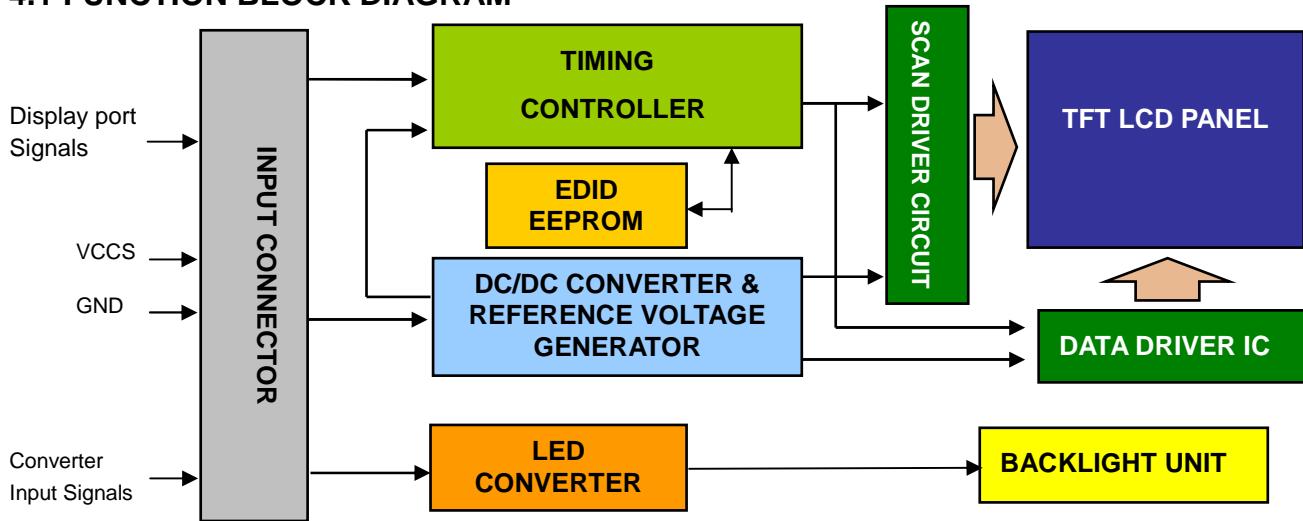
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CCS}	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	V _{CCS} +0.3	V	
Converter Input Voltage	LED_V _{CCS}	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

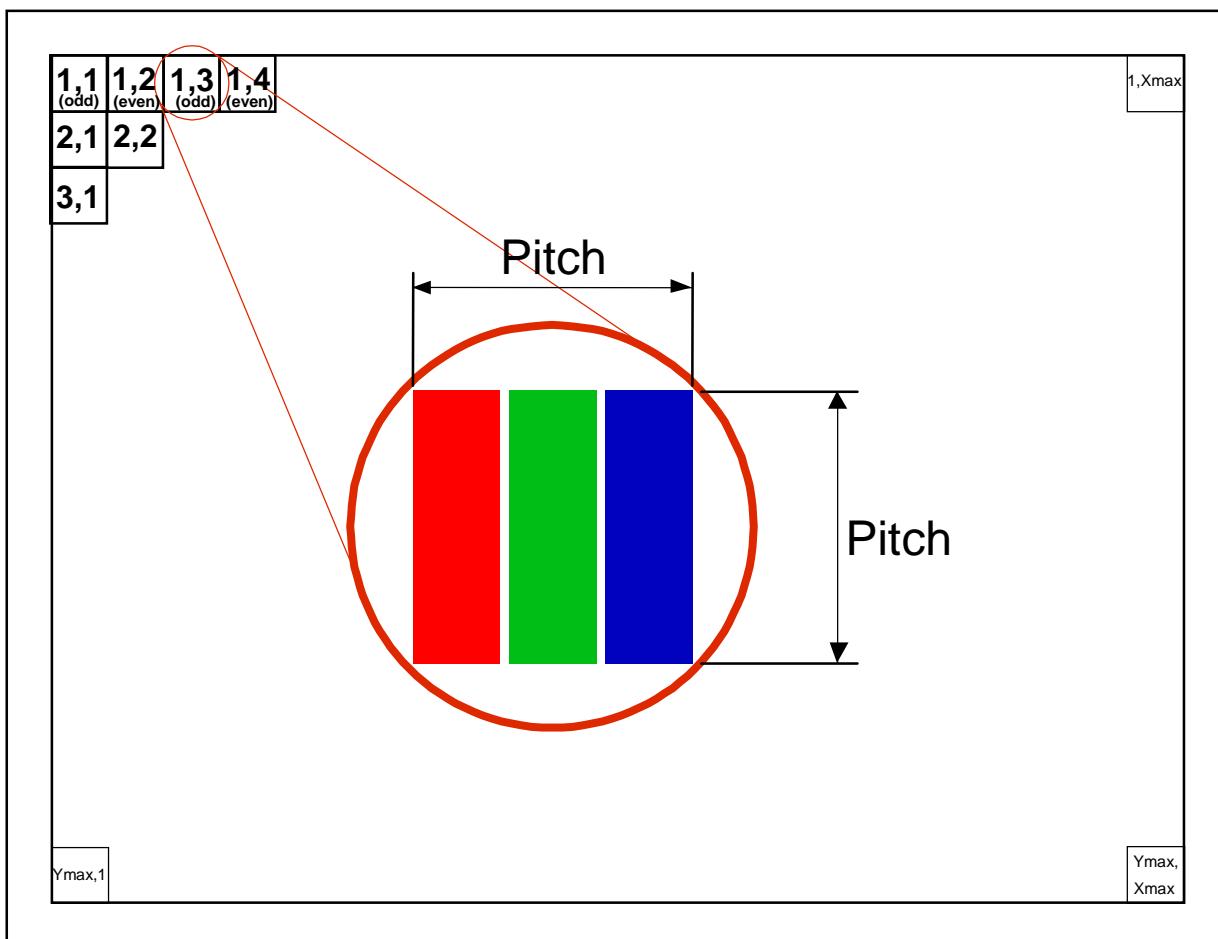
PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	ML1-	Complement Signal-Lane 1	
4	ML1+	True Signal-Main Lane 1	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for LCD test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for LCD test)	
25	NC	No Connection (Reserved for LCD test)	

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26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for LCD test)	

Note (1) The first pixel is odd as shown in the following figure.



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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

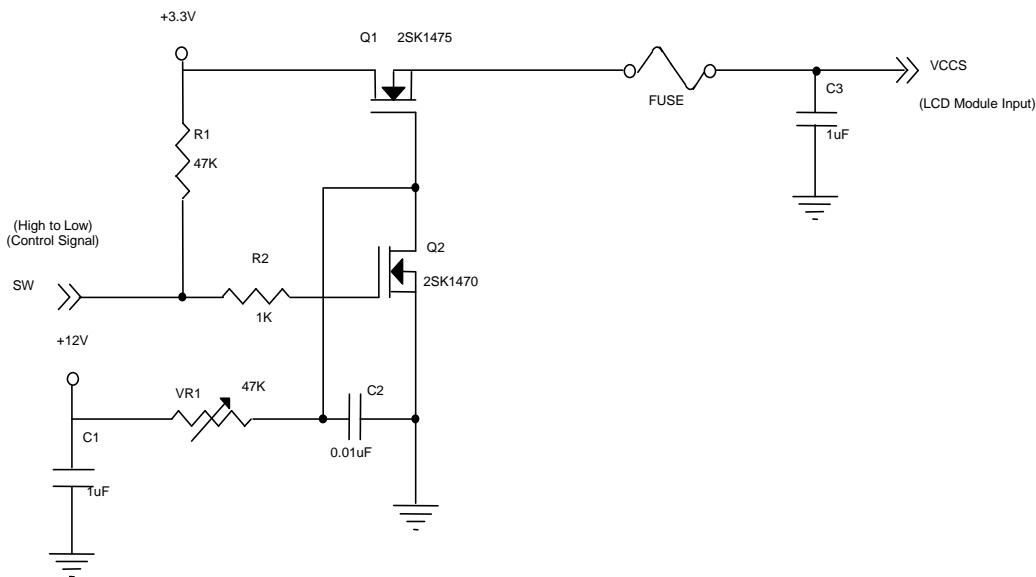
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
HPD	High Level		2.25	-	2.75	V	
	Low Level		0	-	0.4	V	
Ripple Voltage		V _{RP}	-	50	-	mV	(1)-
Inrush Current		I _{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I _{cc}		440	520	mA	(3)a
	Black			550	670	mA	(3)b

Note (1) The ambient temperature is $T_a = 25 \pm 2 ^\circ\text{C}$.

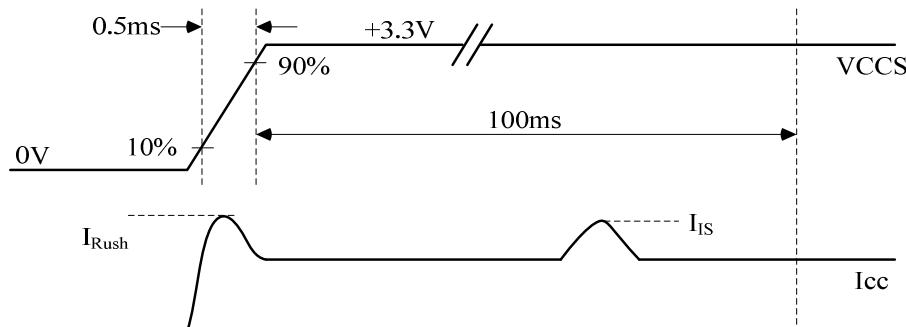
Note (2) I_{RUSH} : the maximum current when VCCS is rising

I_S : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms

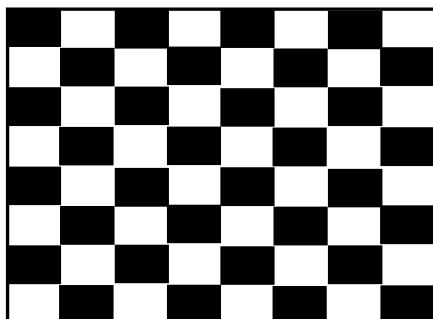


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Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 °C, DC

Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



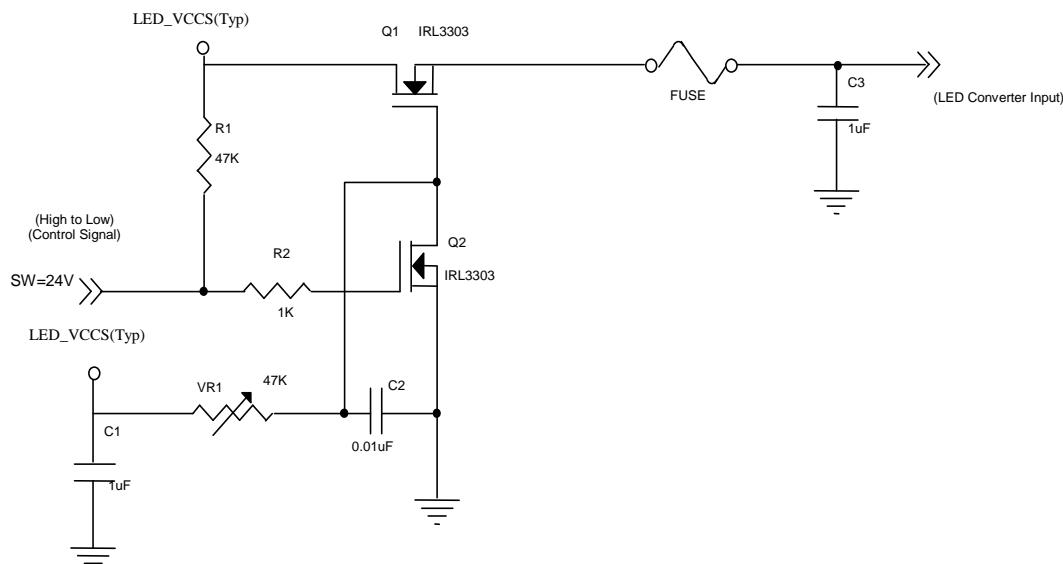
4.3.2 LED CONVERTER SPECIFICATION

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Converter Input power supply voltage	LED_Vccs	7.0	12.0	21.0	V	
Converter Inrush Current	ILED _{RUSH}	-	-	1.5	A	(1)
EN Control Level		2.2	-	5	V	
		0	-	0.6	V	
PWM Control Level		2.2	-	5	V	
		0	-	0.6	V	
PWM Control Duty Ratio		5	-	100	%	
PWM Control Permissive Ripple Voltage	VPWM_pp	-	-	100	mV	
PWM Control Frequency	f _{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS = Typ.	ILED	399	494	571	mA
						(3)

Note (1) ILED_{RUSH}: the maximum current when LED_VCCS is rising,

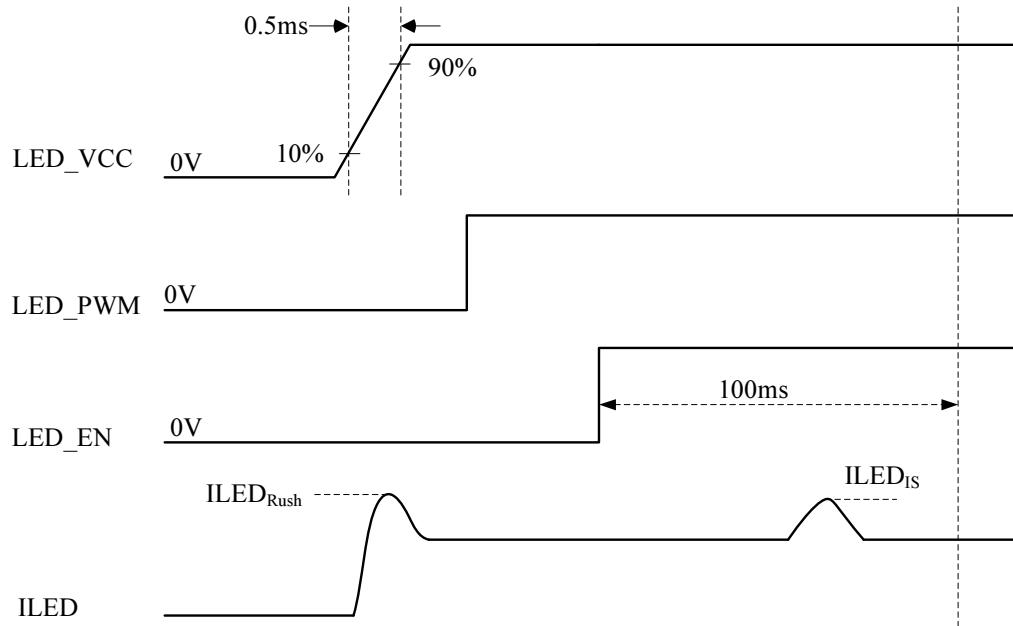
ILED_{IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms

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Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer ($N \geq 3$)

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2 {}^\circ C$, $f_{PWM} = 200$ Hz, Duty=100%.

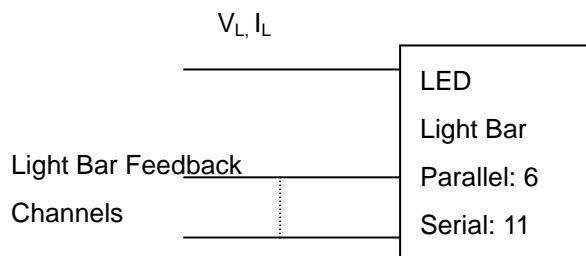
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4.3.3 BACKLIGHT UNIT

 $T_a = 25 \pm 2 {}^\circ C$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	29.7	33	36.4	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L		150		mA	
Power Consumption	P_L		4.95	5.46	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2 {}^\circ C$ and $I_L = 25$ mA(Per EA) until the brightness becomes $\leq 50\%$ of its original value.

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4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

4.4.1 DISPLAY PORT INTERFACE

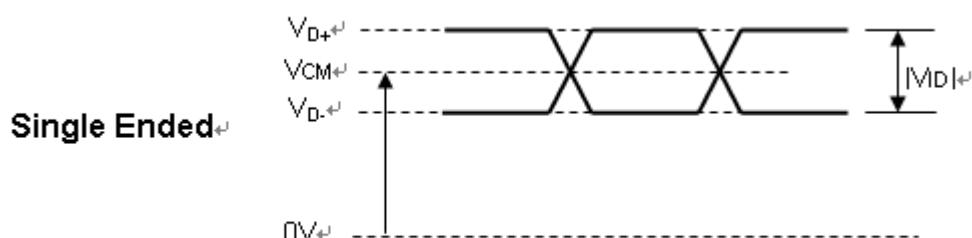
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	V _C M	0		2	V	(1)(3)
AUX AC Coupling Capacitor	C _{AUX}	75		200	nF	(2)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard

Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

(2)The AUX AC Coupling Capacitor should be placed on Source Devices.

(3)The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1



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4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(64)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(64)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Blue(64)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

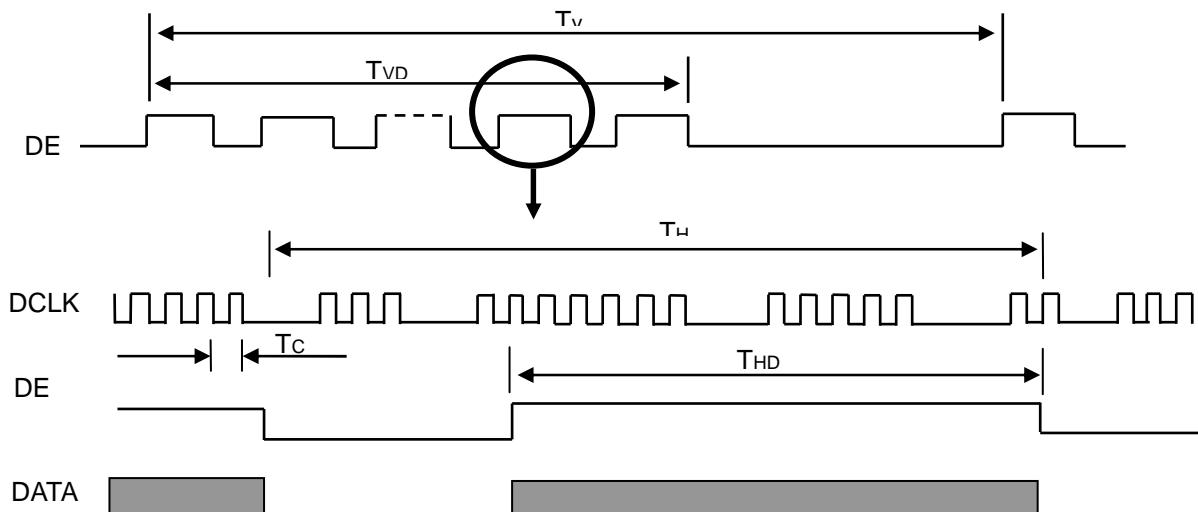
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4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

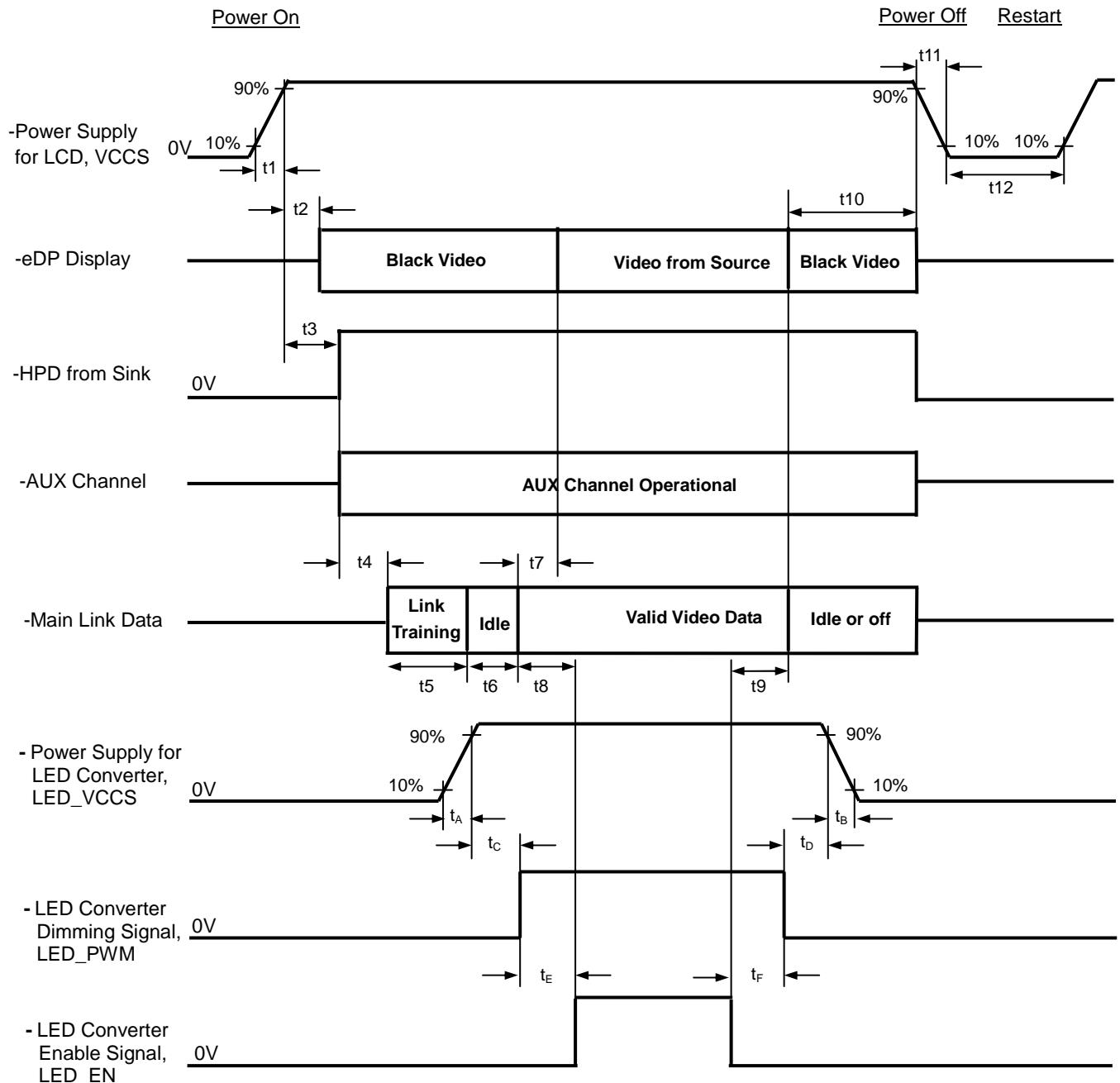
Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	138	152.84	160	MHz	-
	Vertical Total Time	TV	1090	1132	1280	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2120	2250	2620	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	330	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM

4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



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Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	-	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	-	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	-	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	Source must assure display video is stable
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below)
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-

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t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	1	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	1	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from the Source. Black Video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

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5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	150	mA

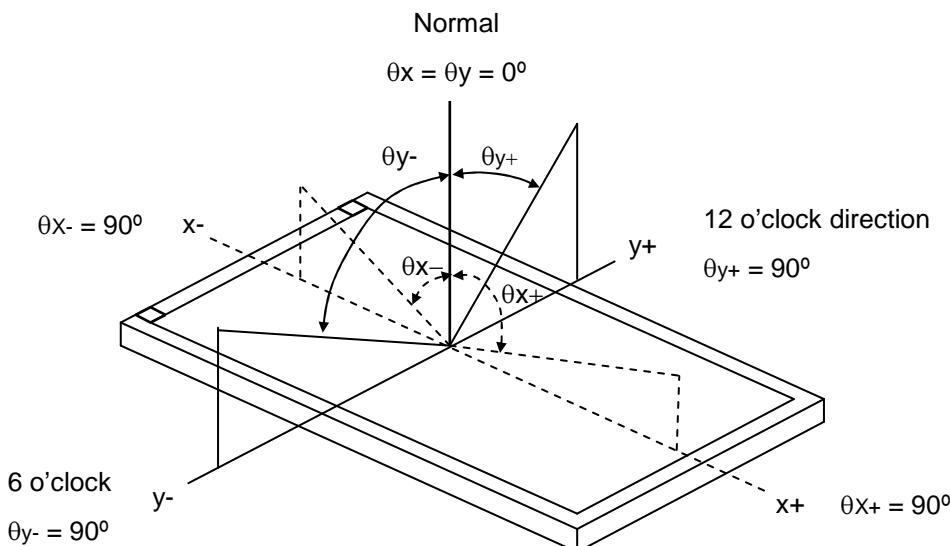
The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio	CR		250	400	-	-	(2), (5),(7)
Response Time	T _R	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	-	2	8	ms	(3),(7)
	T _F		-	6	12	ms	
Average Luminance of White	L _{AVE}		255	300	-	cd/m ²	(4), (6),(7)
Color Chromaticity	Red	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	0.640	Typ + 0.03	-	-	(1),(7)
	Ry		0.333		-	-	
	Green		0.313		-	-	
	Gy		0.613		-	-	
	Blue		0.154		-	-	
	Bx		0.060		-	-	
	By		0.313		-	-	
	White		0.329		-	-	
Viewing Angle	Horizontal	CR≥10	60	70	-	-	(1),(5),(7)
	θ_x+		60	70	-	-	
	θ_x-		50	60	-	-	
	Vertical		50	60	-	-	
White Variation of 5 Points	δW_{5p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	80	-	-	%	(5),(6),(7)

PRODUCT SPECIFICATION

Note (1) Definition of Viewing Angle (θ_x, θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

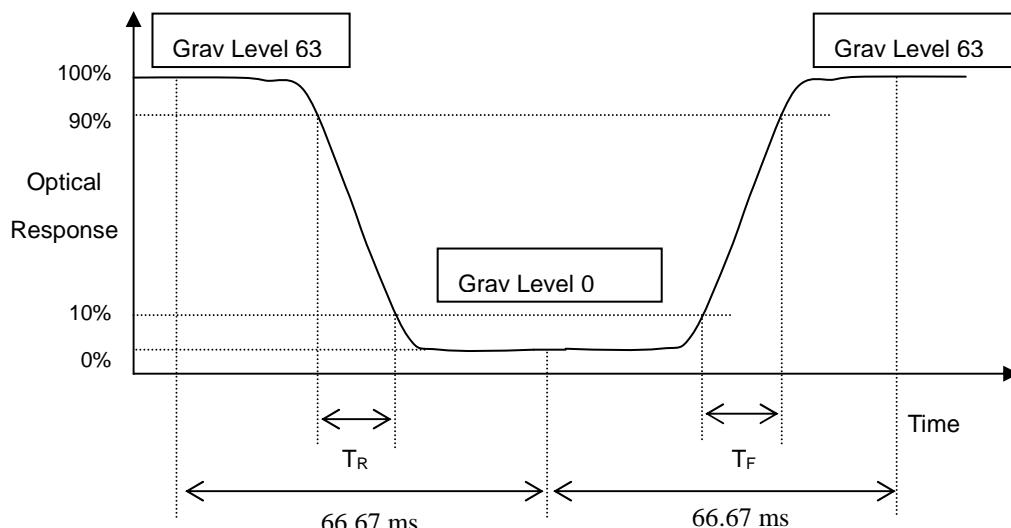
L_{63} : Luminance of gray level 63

L_0 : Luminance of gray level 0

$$CR = CR(1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of White at 5 points

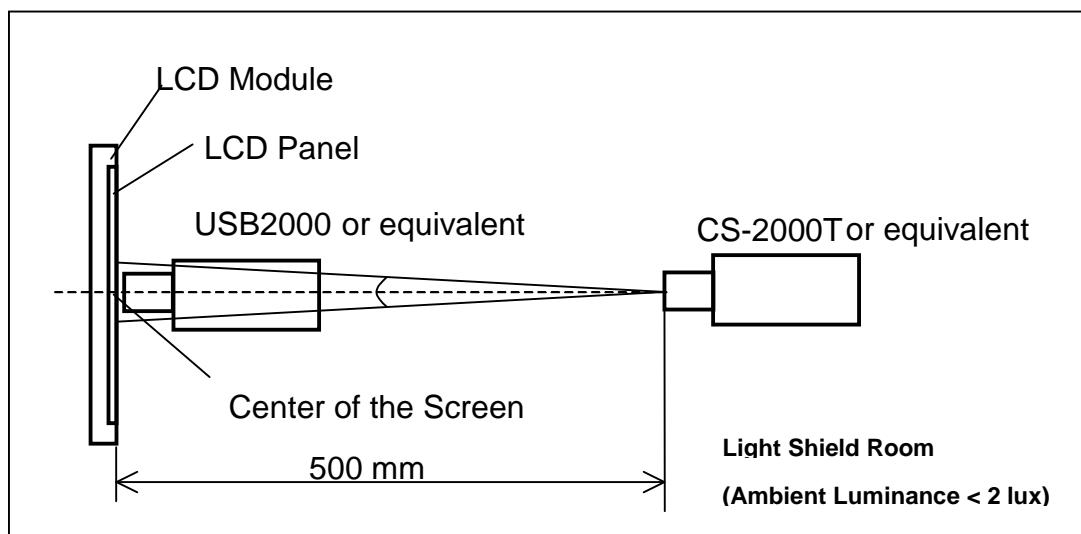
PRODUCT SPECIFICATION

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



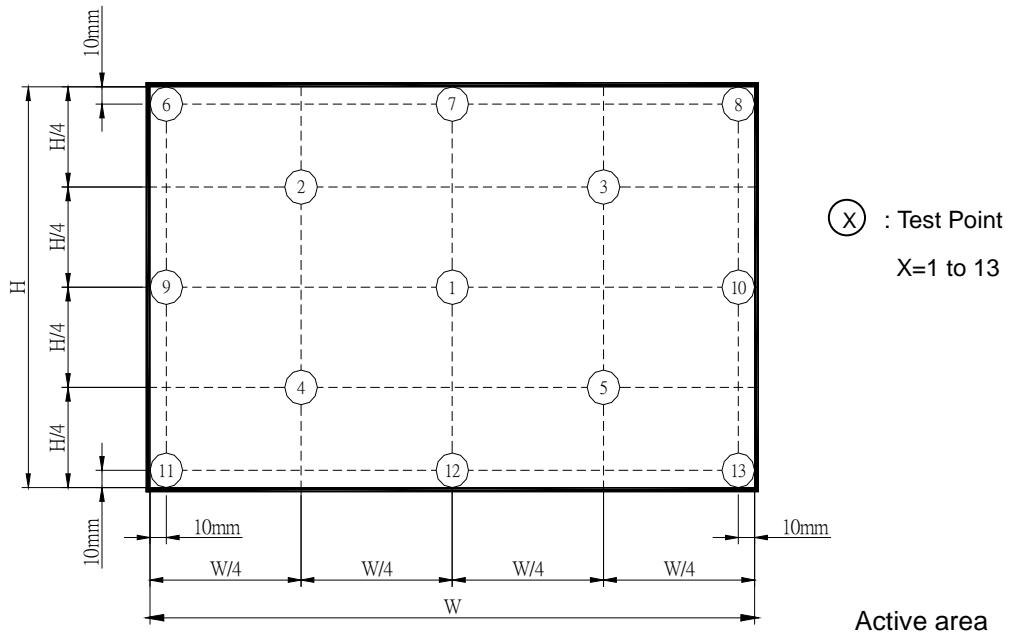
Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points / 13 points

$$\delta W_{5p} = \{ \text{Minimum } [L(1) \sim L(5)] / \text{Maximum } [L(1) \sim L(5)] \} * 100\%$$

$$\delta W_{13p} = \{ \text{Minimum } [L(1) \sim L(13)] / \text{Maximum } [L(1) \sim L(13)] \} * 100\%$$

PRODUCT SPECIFICATION



(X) : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour↔60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

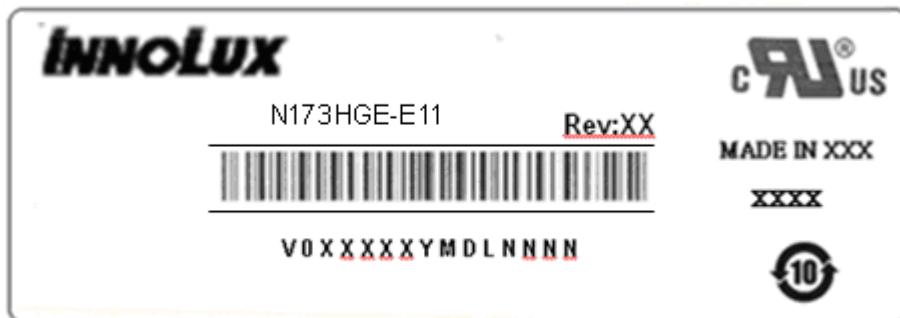
Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING**7.1 MODULE LABEL**

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N173HGE – E11
- (b) Revision: N173HGE-E11 : C1, C2 ...etc.
- (c) Serial ID: X X X X X X X Y M D L N N N N
 - Serial No.
 - Product Line
 - Year, Month, Date
 - INNOLUX Internal Use
 - Revision
 - INNOLUX Internal Use

Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

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7.2 CARTON

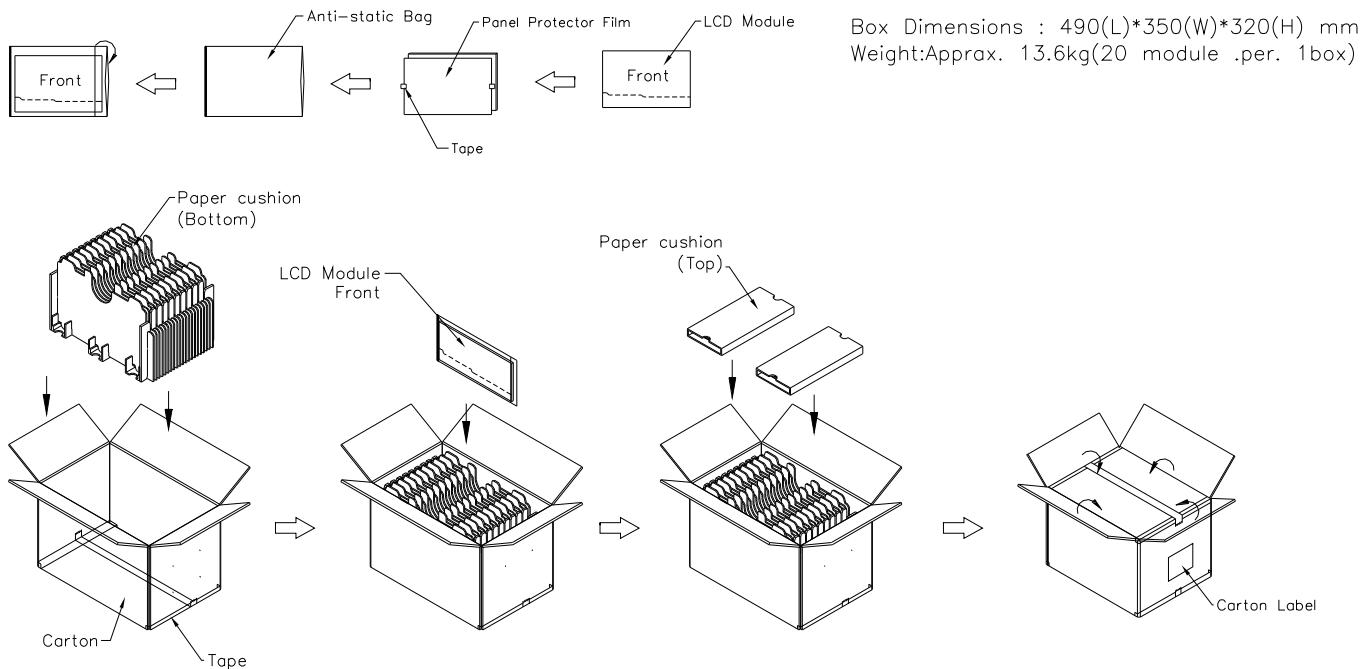
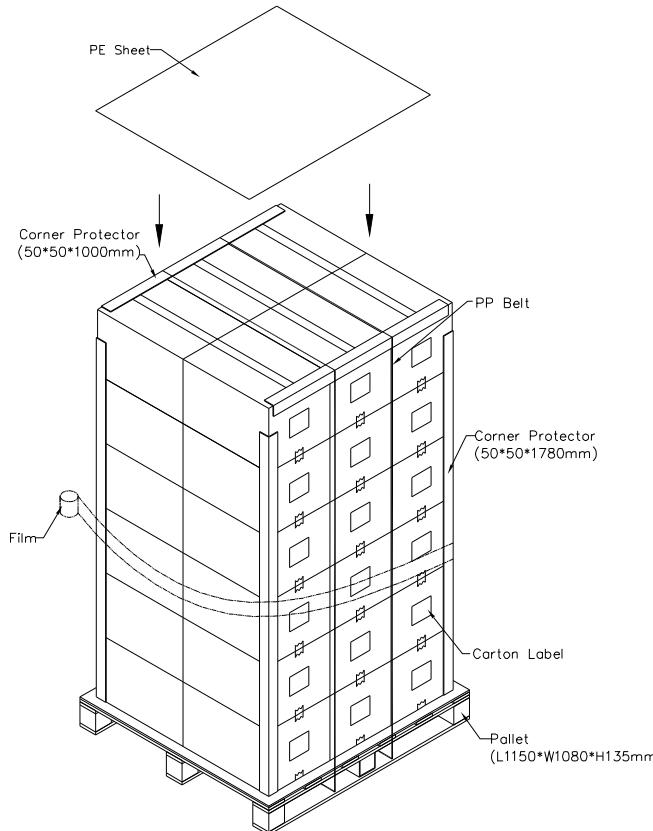


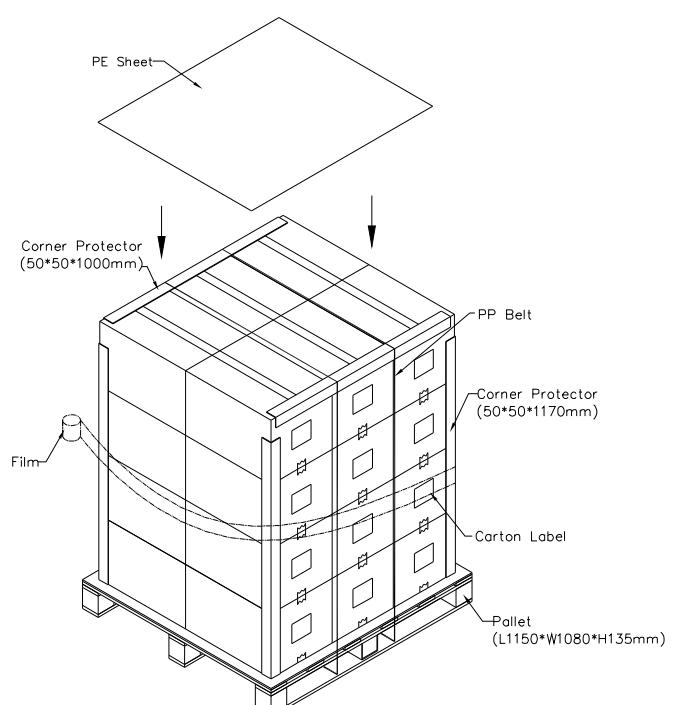
Figure. 7-2 Packing method

7.3 PALLET

Sea & Land Transportation



Air Transportation

**Figure. 7-3 Packing method**

7.4 UN-PACKAGING METHOD

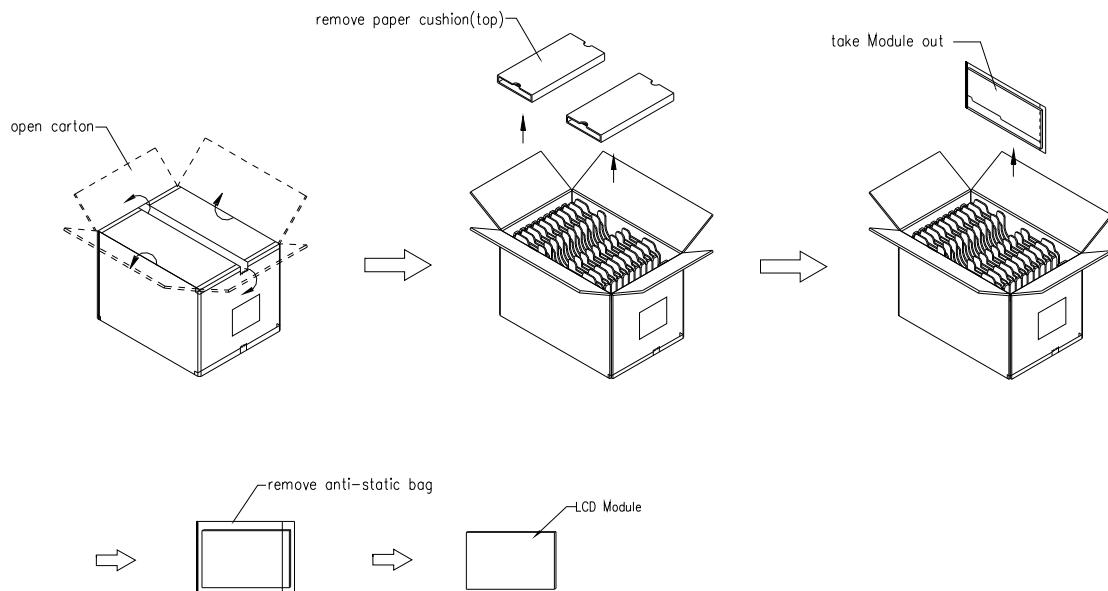


Figure. 7.4 Un-packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

PRODUCT SPECIFICATION

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMN")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
10	0A	ID product code (N173HGE-E11)	35	00110101
11	0B	ID product code (hex LSB first; N173HGE-E11)	17	00010111
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture ("50")	32	00110010
17	11	Year of manufacture ("2012")	16	00010110
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("4")	04	00000100
20	14	Video I/P definition("digital")	95	10010101
21	15	Max H image size ("38cm")	26	00100110
22	16	Max V image size ("21"cm")	15	00010101
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support (Active off, RGB Color)	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	D4	11010100
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.64	A3	10100011
28	1C	Ry=0.333	55	01010101
29	1D	Gx=0.313	50	01010000
30	1E	Gy=0.613	9D	10011101
31	1F	Bx=0.154	27	00100111
32	20	By=0.06	0F	00001111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

PRODUCT SPECIFICATION

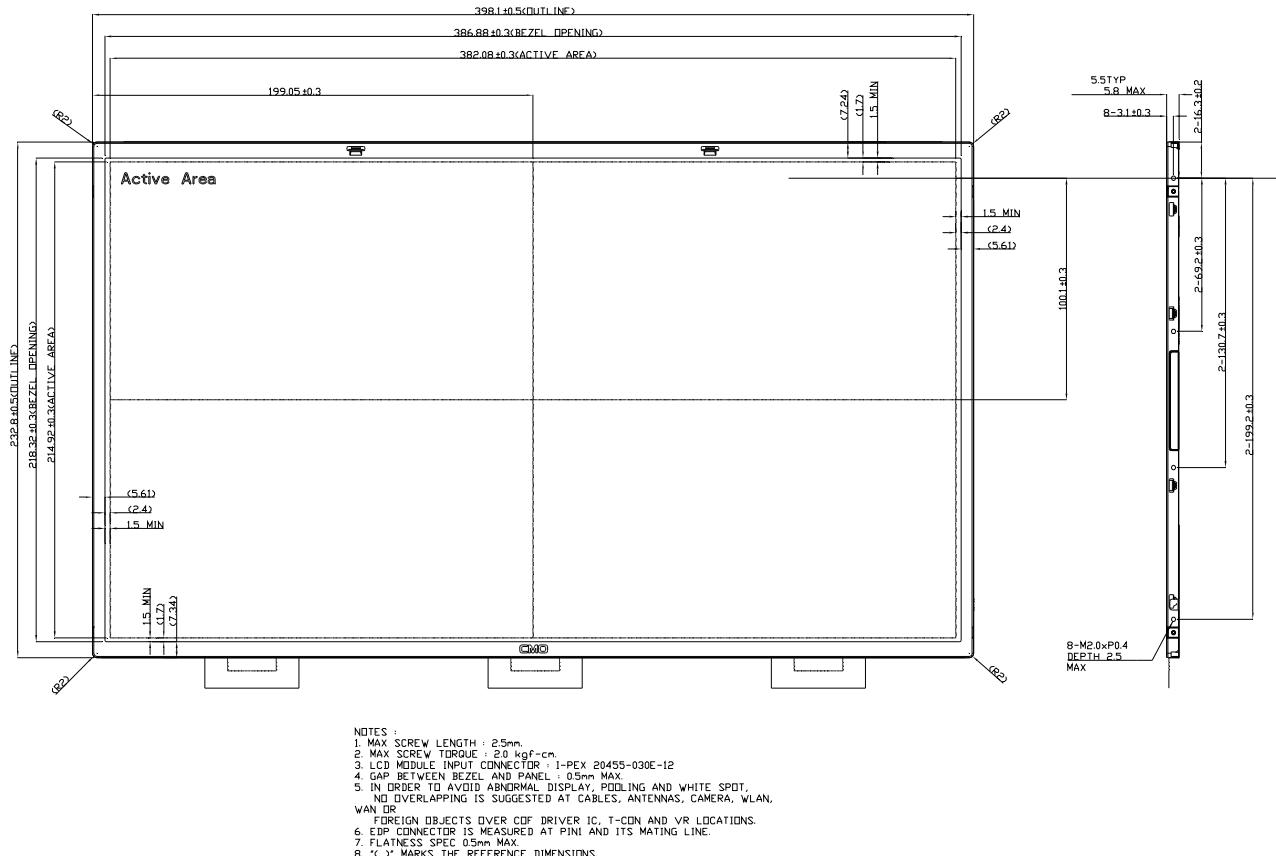
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("152.84"MHz, According to VESA CTV Rev1.4)	B4	10110100
55	37	# 1 Pixel clock (hex LSB first)	3B	00111011
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("330")	4A	01001010
58	3A	# 1 H active : H blank ("1920 : 330")	71	01110001
59	3B	# 1 V active ("1080")	38	00111000
60	3C	# 1 V blank ("52")	34	00110100
61	3D	# 1 V active : V blank ("1080 : 52")	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48 : 32 : 3 : 5")	00	00000000
66	42	# 1 H image size ("382 mm")	7E	01111110
67	43	# 1 V image size ("215 mm")	D7	11010111
68	44	# 1 H image size : V image size ("382 : 215")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N173HGE-E11", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("1")	31	00110001
79	4F	# 2 3rd character of name ("7")	37	00110111
80	50	# 2 4th character of name ("3")	33	00110011
81	51	# 2 5th character of name ("H")	48	01001000
82	52	# 2 6th character of name ("G")	47	01000111
83	53	# 2 7th character of name ("E")	45	01000101
84	54	# 2 8th character of name ("")	2D	00101101
85	55	# 2 9th character of name ("E")	45	01000101

PRODUCT SPECIFICATION

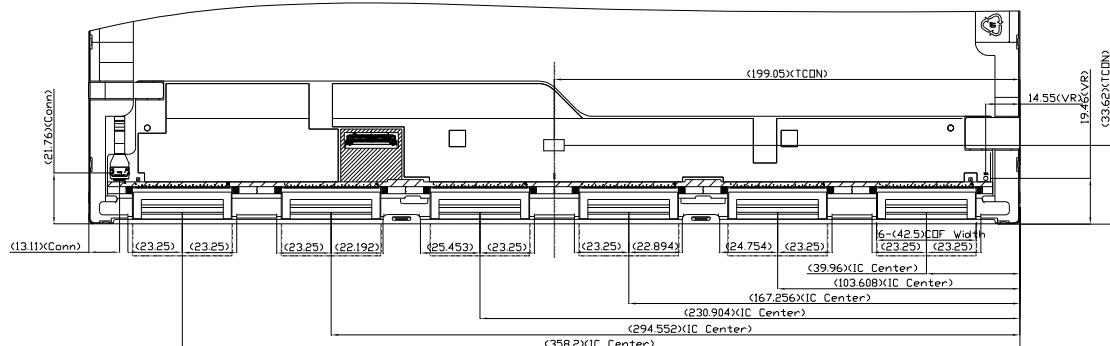
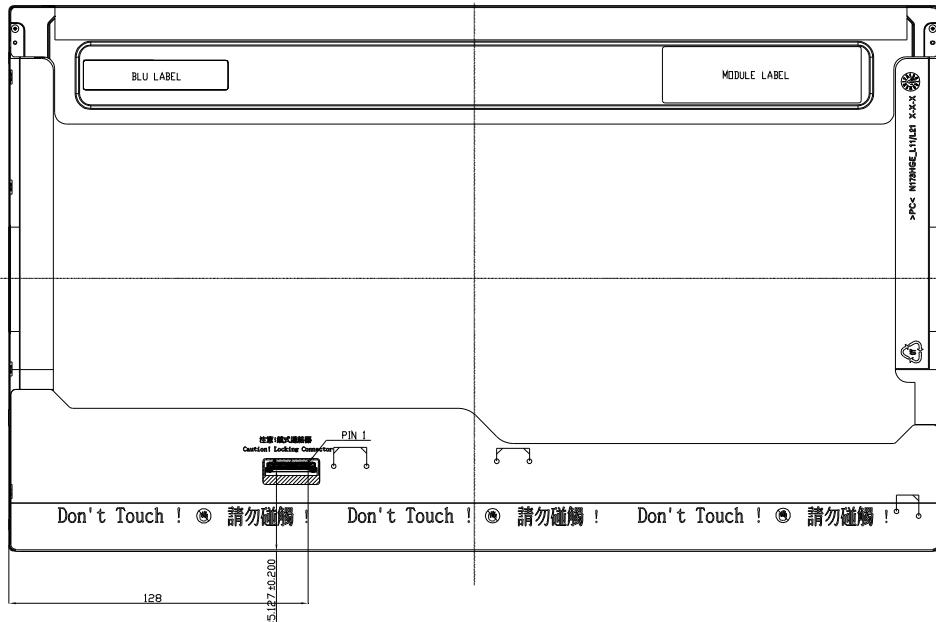
86	56	# 2 10th character of name ("1")	31	00110001
87	57	# 2 11th character of name ("1")	31	00110001
88	58	# 2 New line character indicates end of ASCII string	0A	00001010
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMN", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("N")	4E	01001110
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name "N173HGE-E11", ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name ("N")	4E	01001110
114	72	# 4 2nd character of name ("1")	31	00110001
115	73	# 4 3rd character of name ("7")	37	00110111
116	74	# 4 4th character of name ("3")	33	00110011
117	75	# 4 5th character of name ("H")	48	01001000
118	76	# 4 6th character of name ("G")	47	01000111
119	77	# 4 7th character of name ("E")	45	01000101
120	78	# 4 8th character of name ("")	2D	00101101
121	79	# 4 9th character of name ("E")	45	01000101
122	7A	# 4 10th character of name ("1")	31	00110001
123	7B	# 4 11th character of name ("1")	31	00110001
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	E0	11100000

PRODUCT SPECIFICATION

Appendix. OUTLINE DRAWING



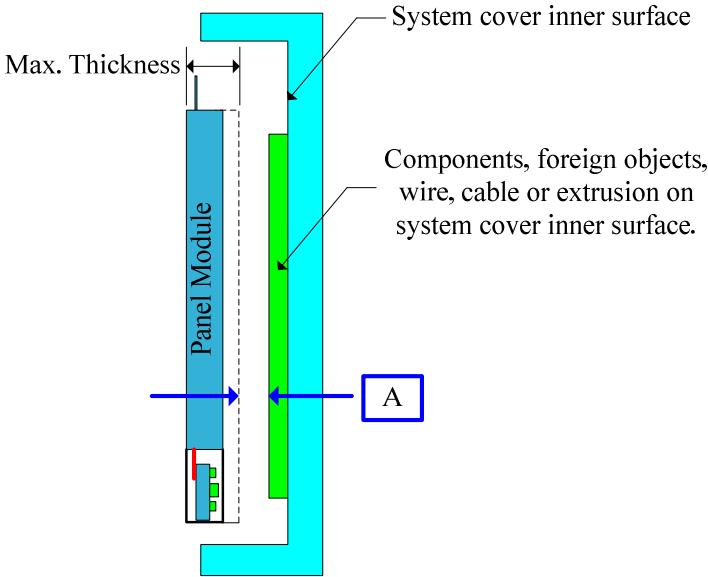
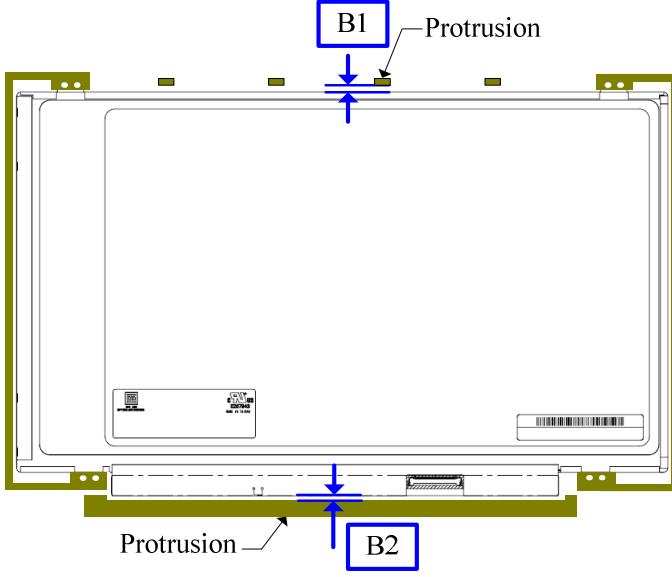
PRODUCT SPECIFICATION



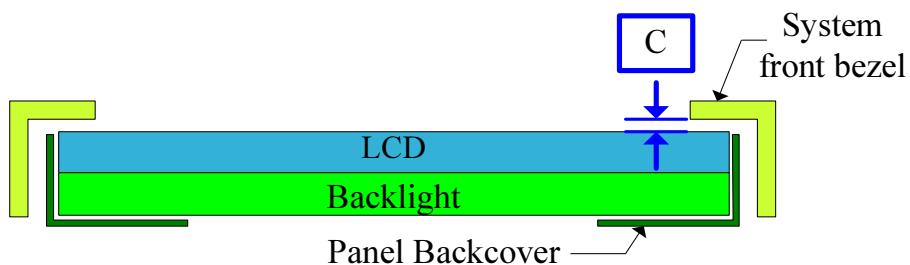
CDF IC, TCON, AND VR
LOCATIONS
SEE NOTE 5 FOR
EXPLANATION.

PRODUCT SPECIFICATION

Appendix. SYSTEM COVER DESIGN NOTICE

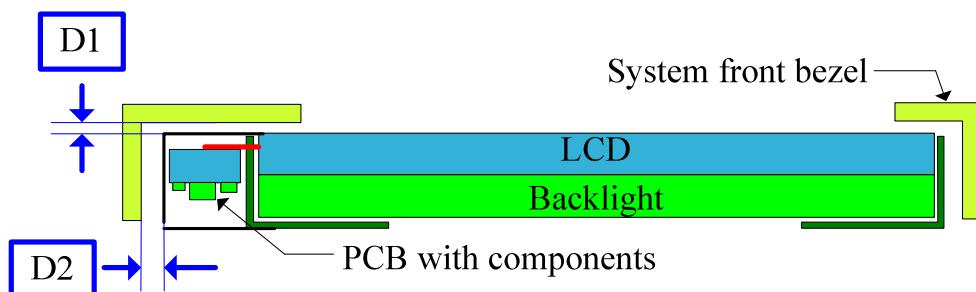
1.	Design gap A between panel & any components on system cover
	
Definition	<p>a). Sufficient gap between panel & system is a must for preventing from backpack or pogo test fail.</p> <p>b). Zero gap from panel's maximum thickness boundary to any components, foreign objects, wire, cable or extrusion on system cover inner surface is forbidden.</p>
2	Design gap B1 & B2 between panel & protrusions
	
Definition	2.0mm min. gap is recommended between panel & protrusions for preventing from shock related failures.
3	Design gap C between system front bezel & panel surface.

PRODUCT SPECIFICATION



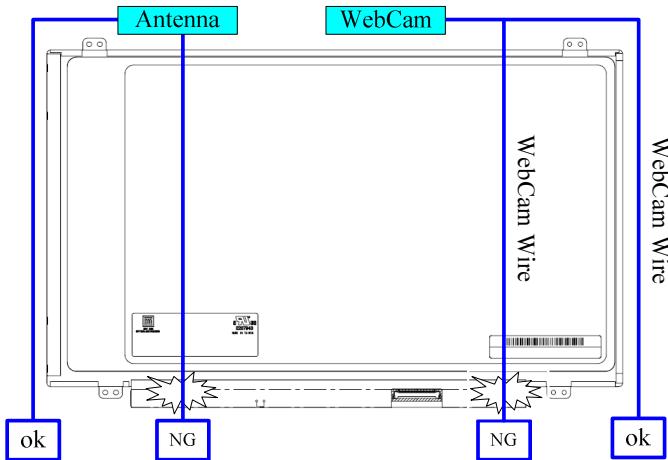
Definition	<ul style="list-style-type: none"> a). Sufficient gap between system front bezel & panel surface is a must for preventing from pooling or glass broken. b). Zero gap or interference is forbidden.
------------	--

4 Design gap D1 & D2 between system front bezel & PCB Assembly.



Definition	<ul style="list-style-type: none"> a). Sufficient gap between system front bezel & PCB assembly is a must for preventing from abnormal display after backpack test, hinge test, twist test or pogo test. b). Zero gap or interference is forbidden.
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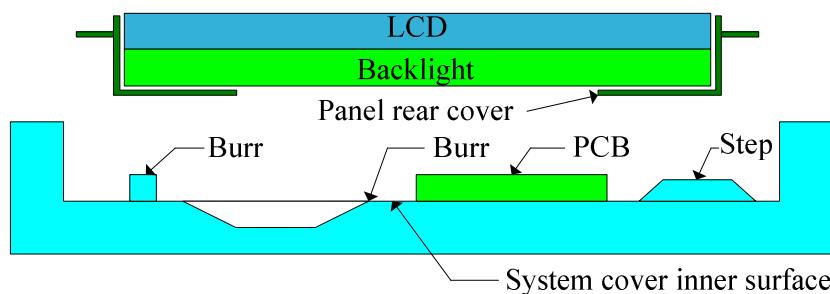
5 Interference examination of antenna cable and WebCam wire



Definition	<ul style="list-style-type: none"> a). Antenna cable or WebCam wire overlap with panel outline is forbidden for preventing from abnormal display & white spot after backpack test, hinge test, twist test or pogo test. b). Antenna cable or WebCam wire bypass panel outline is recommended.
------------	---

6 System inner surface examination

PRODUCT SPECIFICATION



Definition	<ul style="list-style-type: none">a). Burr at logo edge, step, protrusion or PCB board will easily cause white spot or glass broken.b). Keeping flat surface underneath backlight is recommended.
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